# Unit 1 (18 M)

**1.State sampling theorem. 2M**

Ans: SAMPLING THEOREM:
Sampling theorem states that a band-limited signal of finite energy having the highest frequency component fm Hz can be represented and recovered completely from a set of samples taken at a rate of fs samples per second provided that fs ≥ 2fm.
Here fs is the sampling frequency. This theorem is also known as the Sampling Theorem for Baseband or Low-pass Signals.

**2.State Hartley's law and Shannon Hartley's theorem. 4M**

Ans: In information theory, the Shannon–Hartley theorem tells the maximum rate at which information can be transmitted over a communications channel of a specified bandwidth in the presence of noise.
According to Shannon, the bandwidth of the channel and signal energy and noise energy are related by the formula
where
C is channel capacity in bits per second (bps)
W is bandwidth of the channel in Hz
S/N is the signal-to-noise power ratio (SNR). SNR generally is measured in dB using the formula

Effect of S/N on Channel Capacity C:

● If the communication channel is noiseless then N = 0. Therefore, S/N → ∞ and so C also will tend to ∞. Thus the noiseless channel will have an infinite capacity.

Effect of Bandwidth B on Channel Capacity C:

● Consider that some white Gaussian noise is present. Hence (S/N) is not infinite as N ≠ 0. Now as the bandwidth approaches infinity, the channel capacity C does not become infinite because, N =ηB will also increase with the bandwidth B. This will reduce the value of S/N with increase in B,assuming the signal power S to be constant.

**3.Explain any one method of error detection with example. 4M**

ANS: Duplicating each data unit for the purpose of detecting errors is a form of error detection called redundancy. Adding bits for the purpose of detecting errors is called redundancy checking. There are four basic types of redundancy checks:

1. Vertical Redundancy Checking (VRC)

2. Checksum

3. Cyclic Redundancy Checking (CRC)

**METHOD 1:**

**1.VERTICAL REDUNDANCY CHECKING (VRC):**

● Vertical Redundancy Checking (VRC) is the simplest error detection scheme and is generally referred to as Character parity or simply Parity. With character parity, each character has its own error detection bit called the parity bit. Since the parity bit is not actually a part of the character, it is considered as a redundant bit.

● An "n" character message would have n redundant parity bits. Therefore, the number of Error detection bits are directly proportional to the length of the message.

● Parity can be of two types:

1. Odd parity
2. Even parity

In odd parity, the total number of 1's in the entire message should be odd whereas in even parity, the total number of 1's in the message should be even.

● With character parity (VRC), a single parity bit is added to each character to force the total
Number of logic 1's in the character, including the parity bit, to be either an odd number (odd parity) or an even number (even parity).

● For example, the ASCII code for the letter C is 43H or P1000011, where the P bit is the parity bit. There are three logic 1's in this code, not counting the parity bit.

● If odd parity is used, the P bit is made logic 0, keeping the total number of logic 1's at three, which is an odd number.

● If even parity is used, the P bit is made logic 1, making the total number of logic 1's four, which is an even number.

● The main advantage of parity is its simplicity.

**METHOD 2:**
**2.CHECKSUM:**

Checksum is error detection method which is based on the concept of redundancy. The checksum detects all errors involving an odd number of bits and most errors involving an even number of bits.

● Checksum encoder follows the following steps

1. The data unit is divided in to "k" sections each of "n" bits
2. All sections are added to get the sum.
3. The sum is complemented and becomes the checksum.
4. The checksum is send as redundant bits along with the data.

● Checksum decoder/checker follows the following steps

1. The data unit is divided in to "k" sections each of "n" bits
2. All sections are added to get the sum.
3. The sum is complemented.
4. If the result is zero data are accepted otherwise; They are rejected.

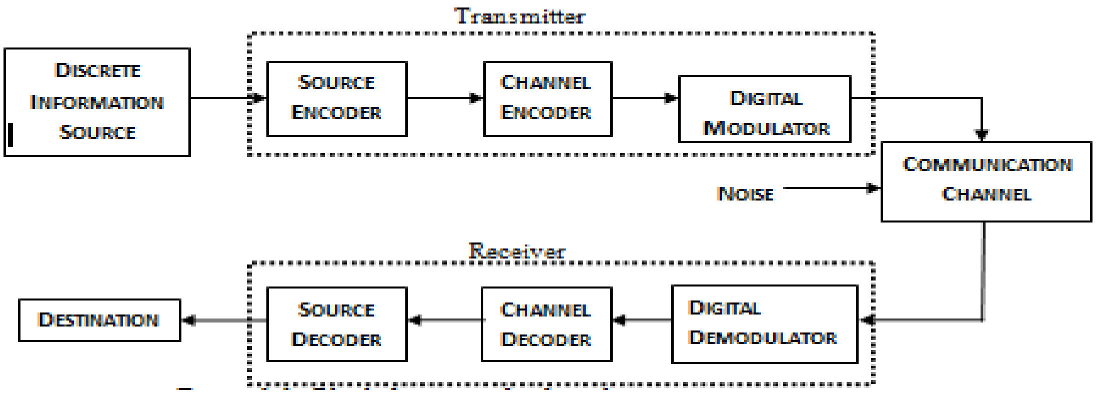
**METHOD 3:**

**3.Cyclic redundancy check:**
CRC is very effective error detection method. It can detect burst errors that affect odd number of bits. Burst error of length less than or equal to the degree of polynomial. CRC is based on binary division. In CRC a sequence of redundant bits called as CRC remainder is appended to the end of the data unit so that the resulting data unit becomes exactly divisible by a second predetermined binary number. At the destination the incoming data unit is divided by the same number (divisor) if at this step there is no remainder the data unit is assumed to be intact and therefore accepted. If the remainder is non zero then the data unit is discarded.
For example data is 100100 and divisor is 1101:
At the transmitter ends.

● String of n zero's is appended to the data unit. The number "n" is 1 less than the number of bits in the predetermined divisor, which is n+ 1 bit.
● The newly elongated data unit is divided by the divisor using binary division. The remainder resulting from this division is the CRC.

## 4. Explain digital communication system with the help of block diagram. 4M

ANS:




**Explanation:-**

**DISCRETE INFORMATION SOURCE:**

 The information to be transmitted originates here. These information/messages may be available in digital form or it may be available in an analog form.

 If it is analog it is sampled and digitized using an A/D converter to make the final source output to be digital in form.

**SOURCE ENCODER :**

 The source encoder therefore reduces the redundancy by performing a one to one mapping of its input bit stream in to another bit stream at its output, but with fewer digits.

 Thus in a way it performs data compression.

**CHANNEL ENCODER:**

 The channel encoder is intended to introduce controlled redundancy into the bit stream at its input in order to provide some amount of error- correction capability to the data being transmitted.

**DIGITAL MODULATOR:**

 The physical channels are basically analog in nature; the digital modulator takes each digital binary digit at its input and maps it, in a one –to – one fashion, into a continuous waveform.

 Binary 'zero' at its input is mapped into a continuous signal so(t) and binary 'one' is mapped into another continuous signal s1(t).

 This is called binary modulation.

**PHYSICAL CHANNEL:**

 The digitally modulated signal is passed on to the physical channel, which is nothing but the physical medium through which the signals are transmitted.

 It may take a variety of forms- a pair of twisted wires, coaxial cable, a wave guide, a microwave radio, or an optical fiber.

**THE DIGITAL DEMODULATOR:**

 The digital demodulator of the receiver receives the noise corrupted sequence of waveforms from the channel and by inverse mapping tries to give at its output, an estimate of the sequence of the binary digits that were available at the input of the digital modulator at the transmitting end.

**THE CHANNEL DECODER:**

 The output sequences of digits from the digital demodulator are fed to the channel decoder. Using its knowledge of the type of coding performed by the channel encoder at the transmitting end and using the redundancy introduced by the channel encoder, it produces as its output, the output of the source coder of the transmitter with as few errors as possible.

**THE SOURCE DECODER**:

 Using its knowledge of the type of encoding performed by the source encoder of the transmitter, the source decoder of the receiver tries to reproduce at its output, a replica of the output of the digital source at the transmitting end.

## 5.Generate CRC code for data word 1101101001 by using divisor as 1101. State two advantages of CRC method. 6M

ANS:

Data word - 1101101001

Divisor - 1101

length of divisor = n bits = 4 bits

Dividend = Data word appended by (n-1) zeros

here n-1 = 4-1 = 3

Dividend = 1101101001000

Carry out division for CRC generation

```
            1000110101
       _________________
1101 )  1101101001000
     ⊕  1101
        00001010
            ⊕ 1101
              01110
             ⊕ 1101
              001110
               ⊕ 1101
                001100
                ⊕ 1101
                 0|001| CRC bits.
```

CRC Code word = Data word appended by CRC bits.

so $\boxed{\text{CRC Code word} = 1101101001001}$

**6.State the advantages and disadvantages of digital communication system. 4M**

**Ans: Advantages of Digital Communication :**

1. High noise interference tolerance due to digital nature of the signal. 2. With channel coding, error detection and correction at receiver is possible. 3. It provides us added security to our information signal i.e. Data encryption is possible for greater security. 4. Cheaper due to advances in digital VLSI technology. 5. Digital information can be saved and retrieved when necessary. 6. Large data storage is possible.

**Disadvantages of Digital Communication :**

1. Large System Bandwidth: - Digital transmission requires a large system bandwidth to communicate the same information in a digital format as compared to analog format. 2. High power consumption (Due to various stages of conversion). 3. Needs synchronization 4.Sampling Error

## 7.Generate the Hamming code for the data (1001101) using even parity. 4M

Ans: Construct the even parity Hamming code word for a data byte 1001101.

The number (1001101) of bits is 7.

The value of r is calculated as −

$$2^R \geq M + R + 1$$

$$\Rightarrow 2^4 \geq 7 + 4 + 1$$

Therefore, the number of redundancy bits = 4

Now, let's calculate the required number of parity bits.

We take $P = 2$, then $2^P = 2^2 = 4$ and $n + P + 1 = 4 + 2 + 1 = 7$

The 2 parity bits are not sufficient for the 4-bit data.

Now, we will take $P = 3$,then $2^P = 2^3 = 8$ and $n + P + 1 = 4 + 3 + 1 = 8$

Therefore, 3 parity bits are sufficient for 4-bit data.

The total bits in the codeword are − 4 + 3 = 7

**Position 1: checks the bits 1,3,5,7,9 and 11.**

? _1_0 0 1_1 0 1 0.In position 1 even parity so set position 1 to a 0:0_1_0 0 1_1 0 1 0.

0 1 0 1 1 0 0 1 0

**Position 2: checks bits 2,3,6,7,10,11.**

0 ? 1_0 0 1_1 0 1 0. In position 2 odd parity so set position 2 to.a 1:0 1 1_0 0 1_1 0 1 0

0 1 0 1 1 0 0 1 1 0

**Position 4 checks bits 4,5,6,7,12.**

0 1 1 ? 0 0 1_1 0 1 0. In position 4 odd parity so set position 4 to.a 1: 0 1 1 1 0 0 1_1 0 1 0

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | | 1 | 0 | 0 | 1 | 1 | 1 | 0 |

**Position 8 checks bits 8,9,10,11,12.**

0 1 1 1 0 0 1 ? 1 0 1 0. In position 8 even parity so set position 8 to.a 1: 0 1 1 1 0 0 1 0 1 0 1 0

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |

**Code Word = 011100101010**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

# Unit 2 (16 M)

**8. Describe slope overload and granular noise in DM system. 4M**

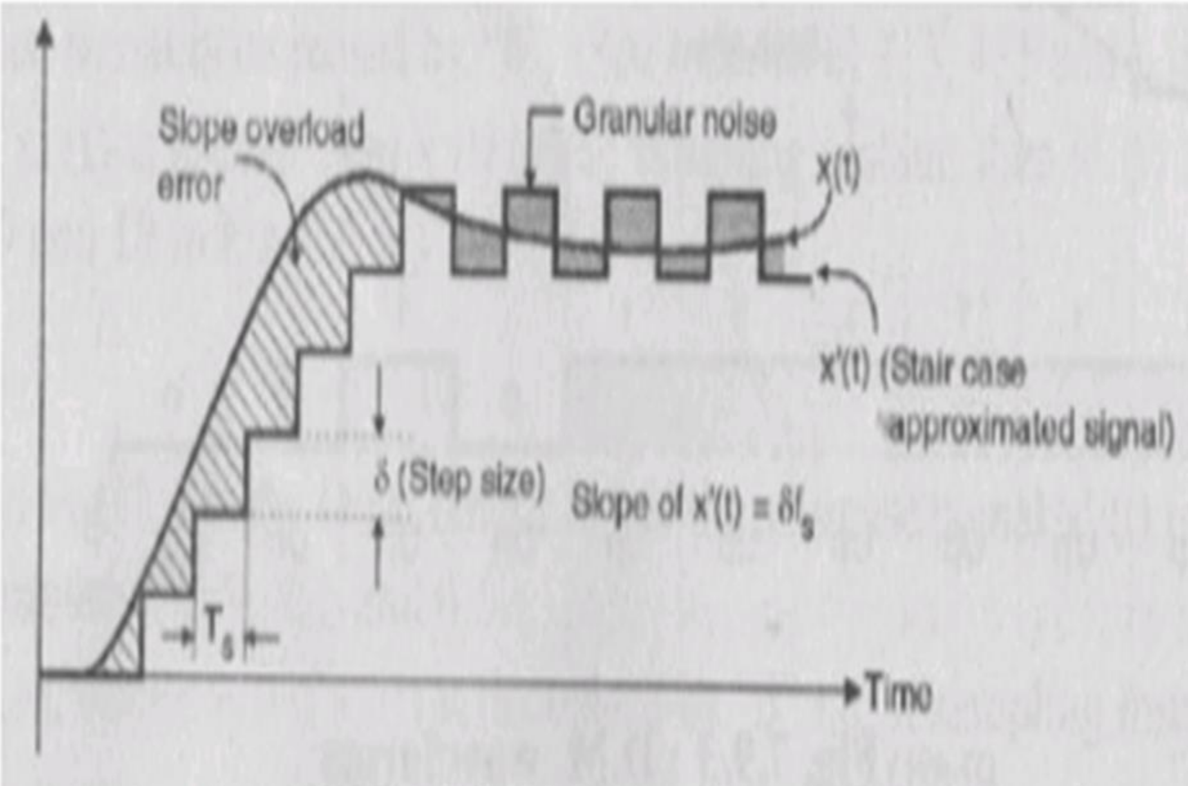
**Ans:**

Increasing step size increases quantization noise. There are two major sources of quantization noise in delta modulation.
a] Slope overload
b] Granular noise.
**a] Slope overload :** When the slope of analog signal is greater than the delta modulator can maintain, it is called slope overload distortion. It is more prevalent in analog s/g that have steep slope or whose amplitude levels vary rapidly.
**b] Granular noise:** When the i/p analog signal has relatively constant amplitude, the reconstructed has variations that were not present in the original s/g. this is called granular noise. Granular noise is more prevalent in analog signal that have gradual slopes and whose amplitude levels vary only by a small amount. It is analogous to quantization noise in conventional PCM.

## Delta modulation has two major drawbacks that are:

1. **Slope overload distortion**
   This distortion arises because of large dynamic range of input signal. To reduce this error, the step size must be increased when slope of signal x(t) is high. Since the step size of delta modulator remains fixed, its maximum or minimum slopes occur along straight lines. Therefore, this modulator is known as Linear Delta Modulator (LDM).
2. **Granular noise**
   Granular noise occurs when step size is too large compared to small variations in the input signal. This means that for very small variations in the input signal, the staircase signal is changed by large amount because of large step size. The error between the input and approximated signal is called granular noise. The solution to this problem is to make step size small. Adaptive Delta Modulation

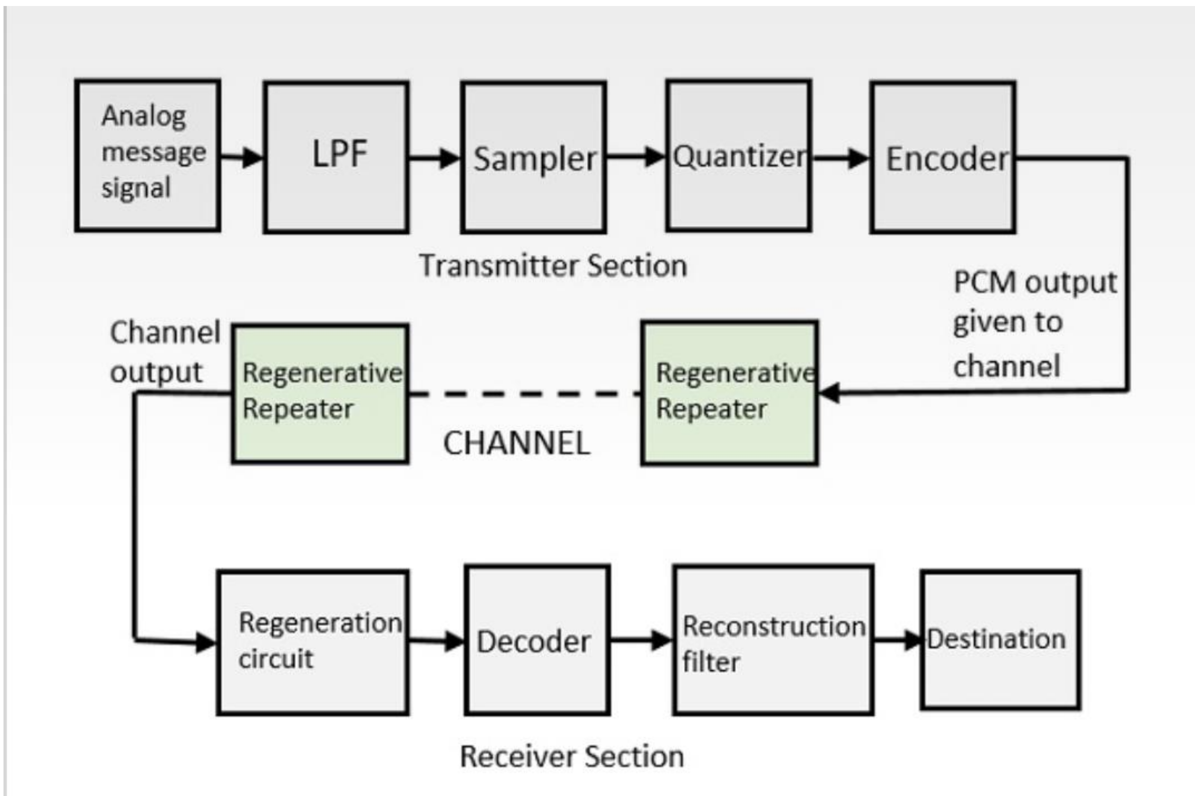
To overcome the quantization error due to slope overload distortion and granular noise, the step size (Δ) is made adaptive to variations in input signal x(t). Particularly in the step segment of the x(t) , the step size is increased. Also, if the input is varying slowly, the step size is reduced. Then this method is known as Adaptive Delta Modulation (ADM). The adaptive delta modulators can take continuous changes in the step size or discrete changes in the step size.




(D-493) Fig. 7.9.5 : Distortions in D.M.

**9. Draw the block diagram of PCM receiver with the help of relevant wave form and explain its working. 4M**

**Ans:**




**1.Low Pass Filter:** This filter removes the high frequency components present in the input analog signal which is greater than the highest frequency of the message signal, to avoid aliasing of the message signal.

**2.Sampler:** This is the technique which helps to collect the sample data at instantaneous values of message signal, so as to reconstruct the original signal. The sampling rate must be greater than twice the highest frequency component W of the message signal, in accordance with the sampling theorem.

**3.Quantizer:** Quantizing is a process of reducing the excessive bits and confining the data. The sampled output when given to Quantizer, reduces the redundant bits and compresses the value.

**4.Encoder:** The digitization of analog signal is done by the encoder. It designates each quantized level by a binary code. The sampling done here is the sample-and-hold process. These three sections (LPF, Sampler, and Quantizer) will act as an analog to digital converter. Encoding minimizes the bandwidth used.

**5.Regenerative Repeater:** This section increases the signal strength. The output of the channel also has one regenerative repeater circuit, to compensate the signal loss and reconstruct the signal, and also to increase its strength.

**6.Decoder:** The decoder circuit decodes the pulse coded waveform to reproduce the original signal. This circuit acts as the demodulator. Demodulator converts digital signal into analog signal.

**7.Reconstruction Filter(LPF):**

- After the digital-to-analog conversion is done by the regenerative circuit and the decoder, a low-pass filter is employed, called as the reconstruction filter to get back the original signal.
- Hence, the Pulse Code Modulator circuit digitizes the given analog signal, codes it and samples it, and then transmits it in an analog form.
- This whole process is repeated in a reverse pattern to obtain the original signal.

**10. Describe the working of an ADM transmitter with neat block diagram. State drawbacks of DM overcome by ADM. 6M**

**Ans:**

- To overcome the quantization errors due to slope overload and granular noise, the step size ($\delta$) is made adaptive to variations in the input signal x(t).
- Particularly in the steep segment of the signal (t), the step size is increased .When the input is varying slowly , the step size is reduced .Then the method is called Adaptive Delta Modulation(ADM).
- The adaptive delta modulators can take continuous changes in step size or discrete changes in step size.
- Fig.1 (a) shows the transmitter and Fig.1 (b) shows receiver of adaptive delta modulator. The logic for step size control is added in the diagram.
- The step size increases or decreases according to certain rule depending on one bit quantizer output .For example if one bit quantizer output is high (1), then step size may be doubled for next sample.

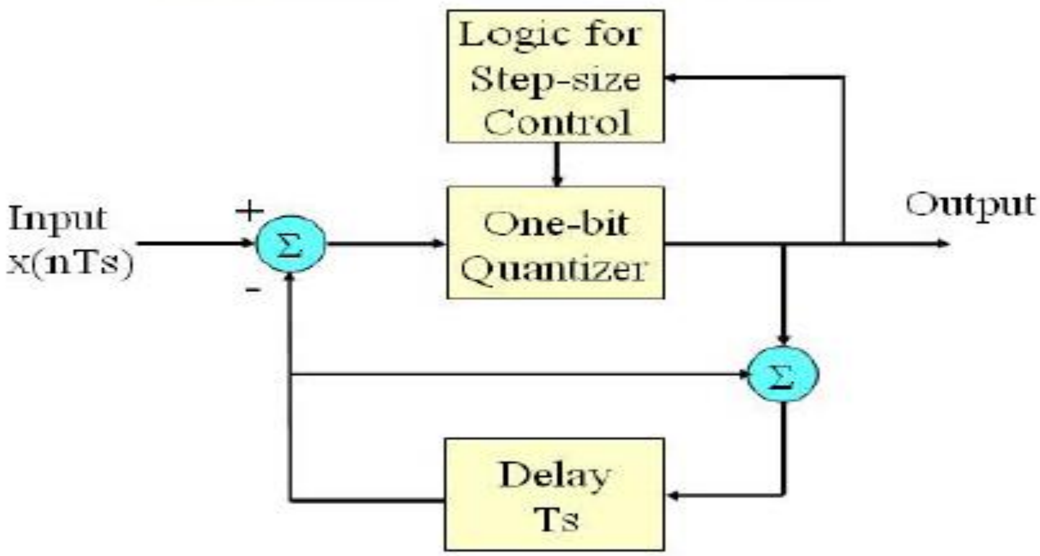



Fig.1(a) Delta modulation transmitter

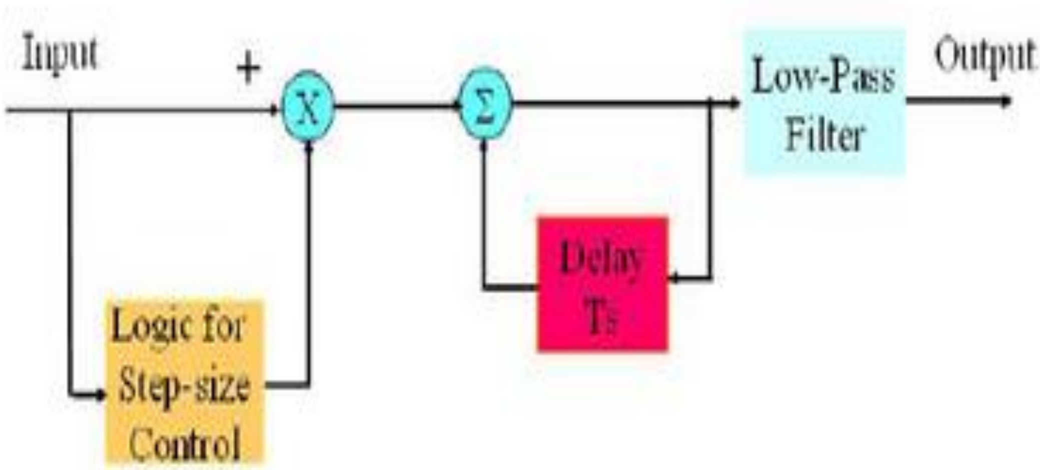



Fig.1(b) Delta modulation receiver

- In the receiver of adaptive delta delta modulator shown in Fig.1(b) the first part generates the step size from each incoming bit. Exactly the same process is followed as that in transmitter.
- The previous input and present input decides the step size. It is then given to an accumulator which builds up staircase waveform.
- The lowpass filter then smoothens out the staircase waveform to reconstruct the smooth signal.
- If one bit quantizer output is low, then the step size may be reduced by one step. Fig.2 shows the waveforms of adaptive delta modulator and sequence of bits transmitted.

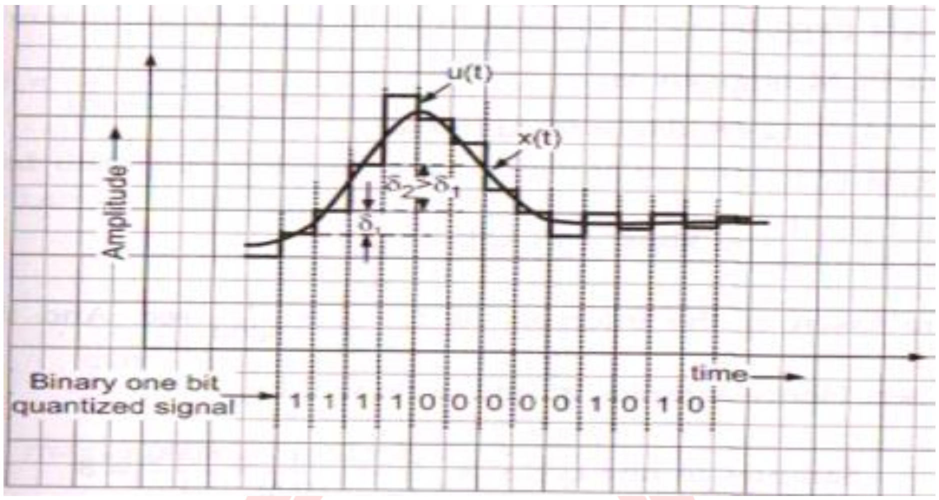


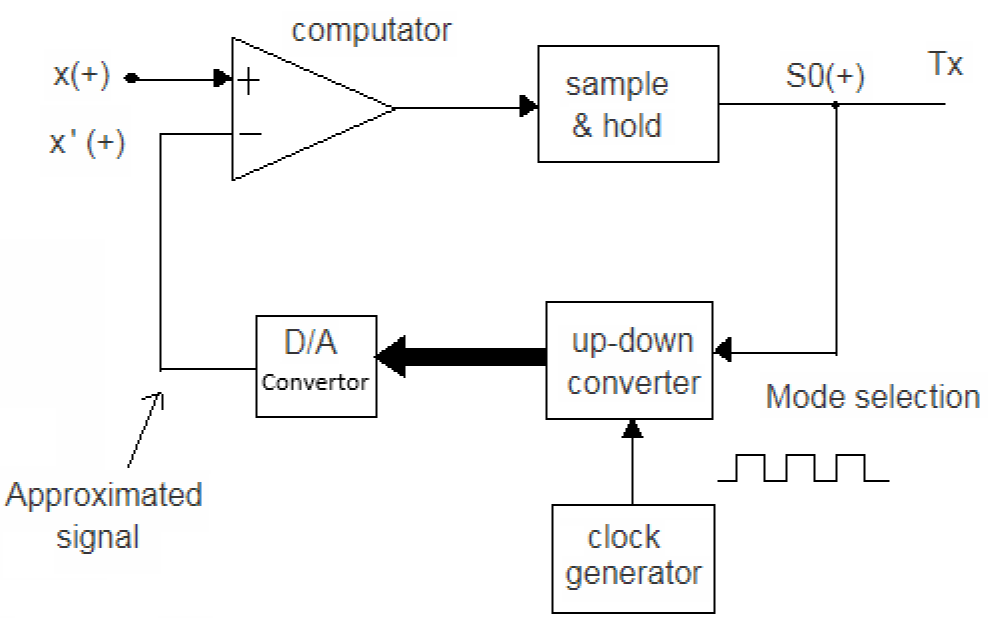

Fig.2 Waveform of adaptive delta modulation

**11. Draw the block diagram of DM transmitter. Explain each block in detail. 4M**

**Ans:**

## Delta modulator Transmitter:

The block diagram of a delta modulation transmitter is as shown below:




**The operation of the circuit is as follows:**

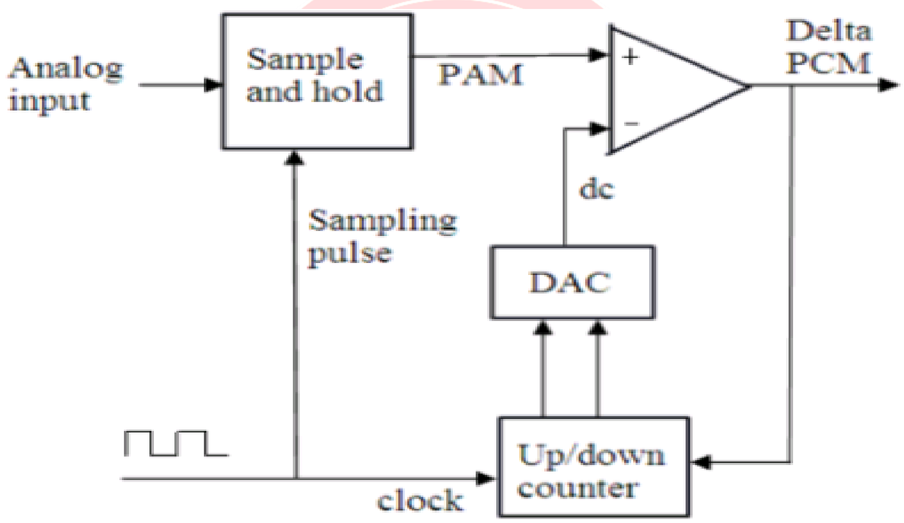
- X(t) is the analog input signal and x'(t) is the quantized version of X(-1). Both these signals are applied to a comparator.
- The comparator o/p goes high and it goes low **if x(t) < x'(t).** Thus the o/p is wither 1 or 0. The sample and hold circuit will hold thus level (0 or 1)

**12. Explain DPCM with block diagram. 4M**

Ans:

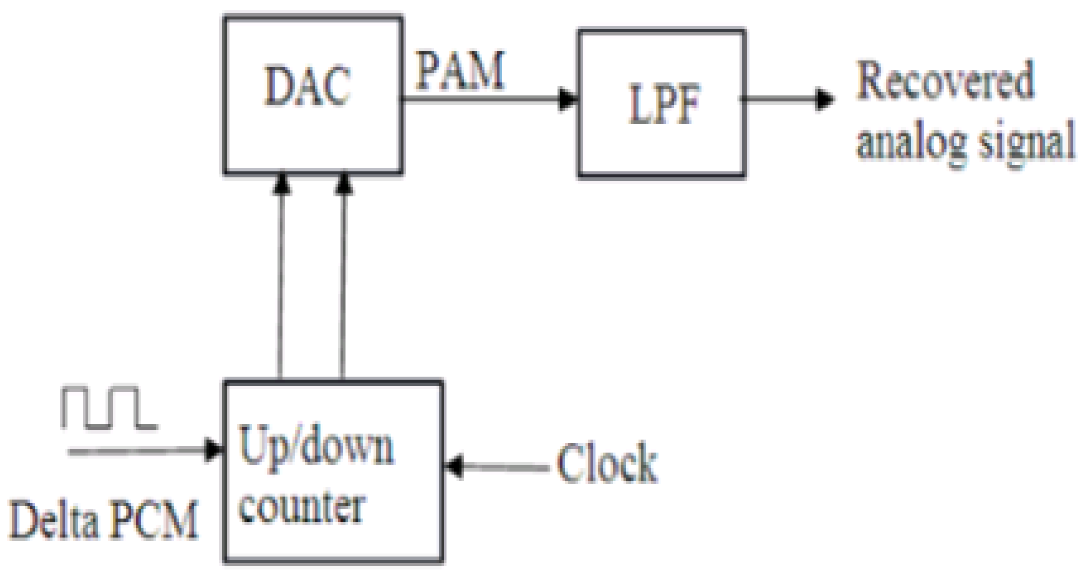
- Delta modulation is a Differential Pulse Code modulation (DPCM) technique in which the difference signal is encoded into a single bit.
- Delta modulation provides a staircase approximation of the input sampled signal where only one bit per sample is transmitted.
- This one bit is sent by comparing the present sample value with the previous sample value and the result whether the amplitude is to be increased or decreased is transmitted.

If the step is reduced, 0 is transmitted and if the step is increased then 1 is transmitted. The Fig1 illustrates the block diagram of Delta modulation transmitter.




- Sample and hold circuit will sample the analog input signal into Pulse amplitude modulated (PAM) signal.
- The generated PAM signal is given as one of the input to the comparator and the other input is a signal from DAC output.
- The Up-down counter stores the magnitude of the previous sample in the binary value.

- This binary number is converted into equivalent voltage in the Digital-to-analog converter (DAC).
- The PAM signal and the DAC output are compared in the comparator, which implies that the sampled signal is compared against the previous sample to increase or decrease the amplitude of the DM signal.
- The Up-down counter is incremented or decremented depending on whether the previous sample is larger or smaller than the current sample.
- This counter is clocked at a rate equal to the sample rate, which is updated after each comparison.
- Depending on the results of comparison, the output of the comparator generates the Delta pulse code modulated signal.
- The Fig2 illustrates the block diagram of Delta modulation receiver.




- The receiver of the delta modulator consists of DAC, up/down counter and LPF. It does not contain the comparator.

- The Delta PCM signal is fed to the up/down counter which works at the same sample rate as transmitter.
- Depending on the binary input received the value in the up/down counter is accordingly incremented or decremented.
- Based on the input received from the up/down counter, DAC will generate the output PAM signal.
- The output signal of DAC in the transmitter and receiver is identical to reconstruct the signal.
- This signal is then allowed to pass through a low pass filter which will filter out the high frequency components from the signal and thus produce the original analog signal.

**Advantages-**

- DPCM can achieve better compression of data compared to standard PCM because it doesn't need to transmit the full sample value for each data point.
- Transmitting only the difference between consecutive samples reduces the data rate, making it suitable for applications with limited bandwidth or storage capacity.
- DPCM can handle linear trends or slowly changing components in the analog signal efficiently.
- DPCM can use the quantization error from the previous sample to predict the quantization error for the current sample

**Disadvantages-**

- DPCM is more sensitive to transmission errors than PCM.
- If there are errors in the transmission or quantization of a few samples, these errors can accumulate, leading to a significant distortion in the reconstructed signal over time.
- DPCM systems can be more complex than standard PCM systems.
- DPCM is most effective when there is a high correlation between consecutive samples.

**13. Compare PCM & DPCM on the basis of following parameters: 4M**

**(1)No. of bits per sample**

**(2) Step size**

**(3)Distortions**

**(4) Feedback from o/p**

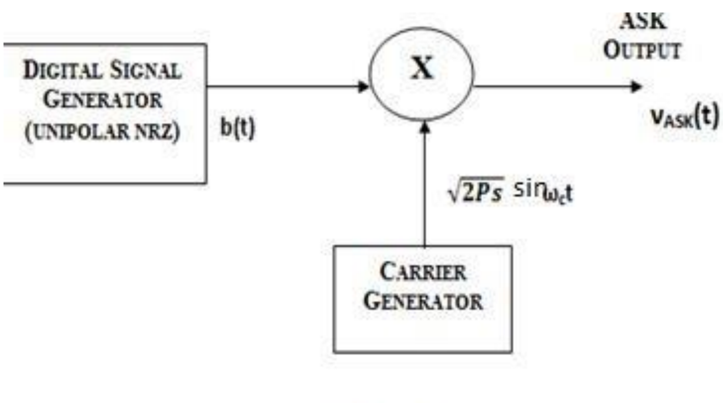
**Ans:**

| **Pulse Code Modulation** | **Delta Modulation** |
|---|---|
| The sampler can use 4, 8, or 16 bits per sampled data. | Only one bit is used per sample. |
| Pulse Code Modulation requires the highest transmitter bandwidth. | Delta Modulation requires the lowest transmitter bandwidth. |
| Pulse Code Modulation is complex. | Delta modulation is simple. |
| Pulse Code Modulation has a good signal-to-noise ratio. | Delta Code Modulation has a poor signal-to-noise ratio. |
| In Pulse Code Modulation, the signal requires an encoder and decoder on both sides. | In Delta Modulation, signals can modulate and demodulate. |
| Pulse Code Modulation is mostly used in video and audio telephony. | Delta Modulation is mostly used for speeches and images. |

# Unit 3 (16 M)

**14. Describe generation of BASK signal with the help of block diagram. 4M**

**Ans:**



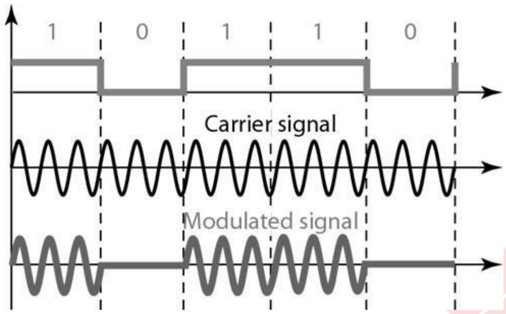

*ASK Transmitter*

**Explanation of ASK Transmitter**

- The ASK technique of binary modulation is illustrated in Figure where modulating signal consists of unipolar pulses.
- Because in this case the carrier is switched ON and OFF, this method is also known as *ON-OFF keying*.
- For the entire time the binary input is high, the output is a constant amplitude, constant frequency signal and for the entire time the binary input is low, the carrier is off.
- Ps is signal power given by $(\text{Amplitude})^2/2$
- ASK is given by:

- $v_{ASK}(t) = b(t)\sin\omega_c t$

**WAVEFORM:**




**15. Describe the M-ary PSK encoding technique with neat block diagram and also draw constellation diagram of BPSK, QPSK. 6M**

**Ans:**

The word binary denotes two-bits. M just denotes a digit that resembles to the number of conditions, levels, or combinations possible for a given number of binary variables. ϖ This is the type of digital modulation method used for data transmission in which in its place of one-bit, two or more bits are transmitted at a time. As a single signal is used for multiple bit transmission, the channel bandwidth is reduced. M-ary Equation ϖ If a digital signal is given below four situations, such as voltage levels, frequencies, phases and amplitude, then M = 4. ϖ The number of bits essential to create a given number of conditions is expressed mathematically as N=log2M ϖ Where, N is the number of bits necessary. M is the number of conditions, levels, or combinations possible with N bits. The above equation can be re-arranged as − 2 N = M ϖ For instance, with two bits, 22 = 4 conditions are possible.

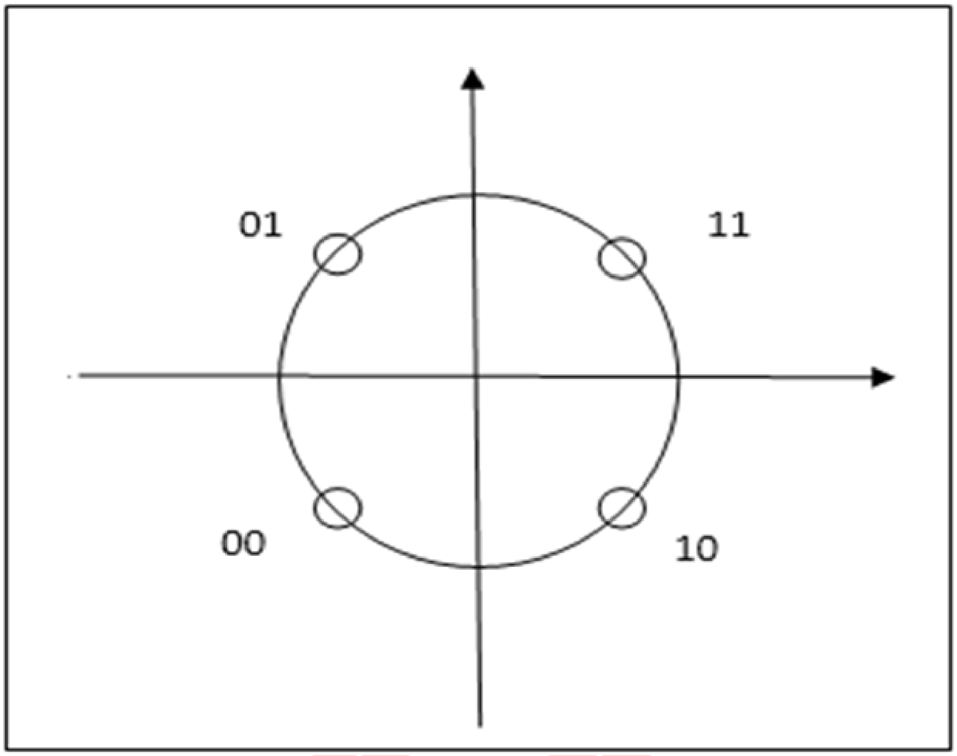



**Fig. Constellation diagram for QPSK Each adjacent symbol only differs by one bit**

**16. Describe amplitude shift keying (ASK) modulation with suitable circuit diagram. 4M**

**Ans:**

**ASK system**:

ASK is a digital modulation technique defined as the process of shifting the amplitude of the carrier signal between two levels , depending on whether 1 or 0 is to be transmitted .

Let the message be binary sequence of 1’s and 0’s . It can be represented as a function of the time as follows :

- **vm=Vm  when symbol is 1**
- **=0 when symbol is 0**

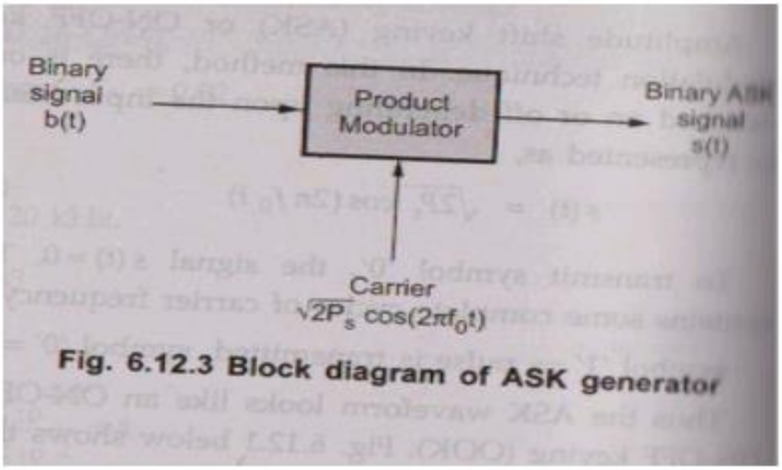
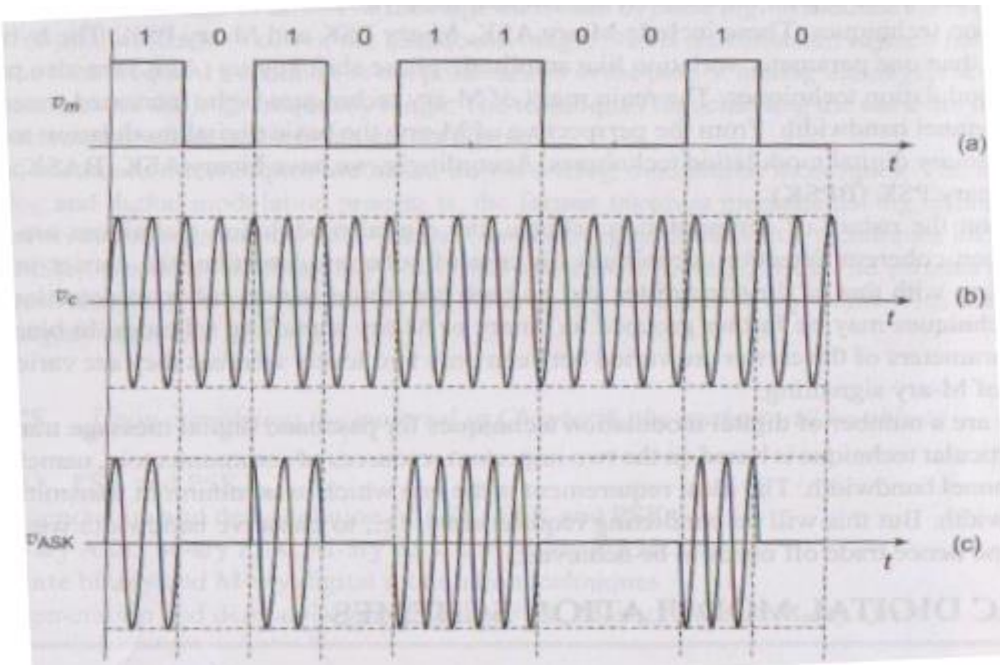


Fig. 6.12.3 Block diagram of ASK generator




Time domain representation of generation of ASK signal (a)message ( b)carrier ( c)ASK signal.

Let the carrier be defined as

vc=Vc cos wct

The corresponding ASK signal is given by the product of vm

and vc

as

vASK=Vm Vc coswct when symbol is 1

=0 when symbol is 0

**17. Compare binary ASK, FSK &PSK modulation techniques (any six points). 6M**

**Ans:**

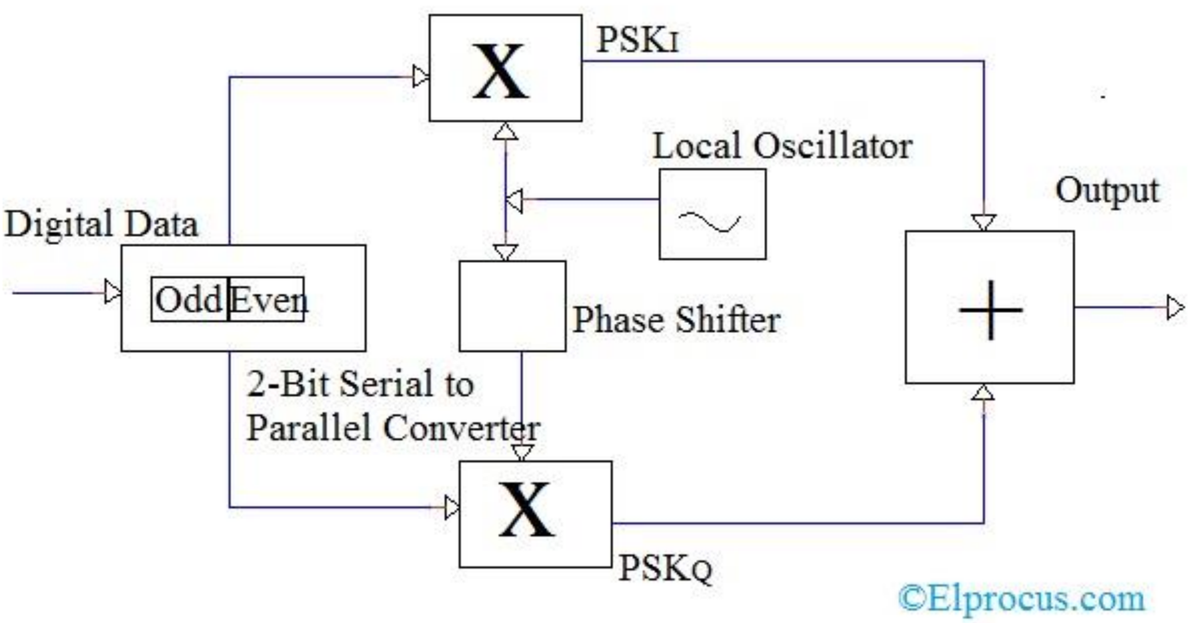
| **ASK** | **FSK** | **PSK** |
|---|---|---|
| 1] Information is in amplitude variations. | Information is in frequency variations. | Information is in phase variations. |
| 2] Less Bandwidth as compared. | More Bandwidth as compared. | Less to moderate Bandwidth. |
| 3] Poor Noise immunity. | Better Noise immunity. | Better Noise immunity. |
| 4] Synchronization is not required. | Synchronization is not required. | Synchronization is essential. |
| 5] Effect of DC is more. | Effect of DC component is less. | Effect of DC component is less. |
| 6] More power required. | Moderate power required. | Less-moderate power required. |
| 7] Low bit rate application | Moderate bit rate application. | High bit rate application. |
| 8] Simple Implementation. | Moderately complex Implementation. | Very complex Implementation. |

**18. Explain QPSK transmitter with block diagram its constellation diagram. 6M**

**Ans:**

Instead of converting bits into a digital stream, QPSK converts it into bit pairs. This method is also known as the Double Side Band Suppressed Carrier modulation method.

QPSK modulation circuit consists of a bit-splitter, 2-bit serial to parallel converter, two multipliers, a local oscillator, and a summer.




- At the transmitter input, the message signal bits are separated as even bits and odd bits using a bit splitter.
- These bits are then multiplied with the same carrier waveform to generate Even QPSK and Odd QPSK signals.

- The Even QPSK signal is phase shifter by 90°, using a phase shifter, before modulation. Here, the Local Oscillator is used for generating the carrier waveform.
- After separation of bits, a 2-bit serial to parallel converter is used.
- After multiplying with the carrier waveform, both Even QPSK and Odd QPSK are given to the summer when modulation output is obtained.
- At the receiver end for demodulation, two product detectors are used. This product detectors convert the modulated QPSK signal into Even QPSK and Odd QPSK signals. Then the signals are passed through two bandpass filters and two integrators. After processing the signals are applied to the 2-bit parallel- to-series converter, whose output is the reconstructed signal.

**19. Distinguish between m-ary PSK & m-ary FSK techniques. (Any six points) 6M**

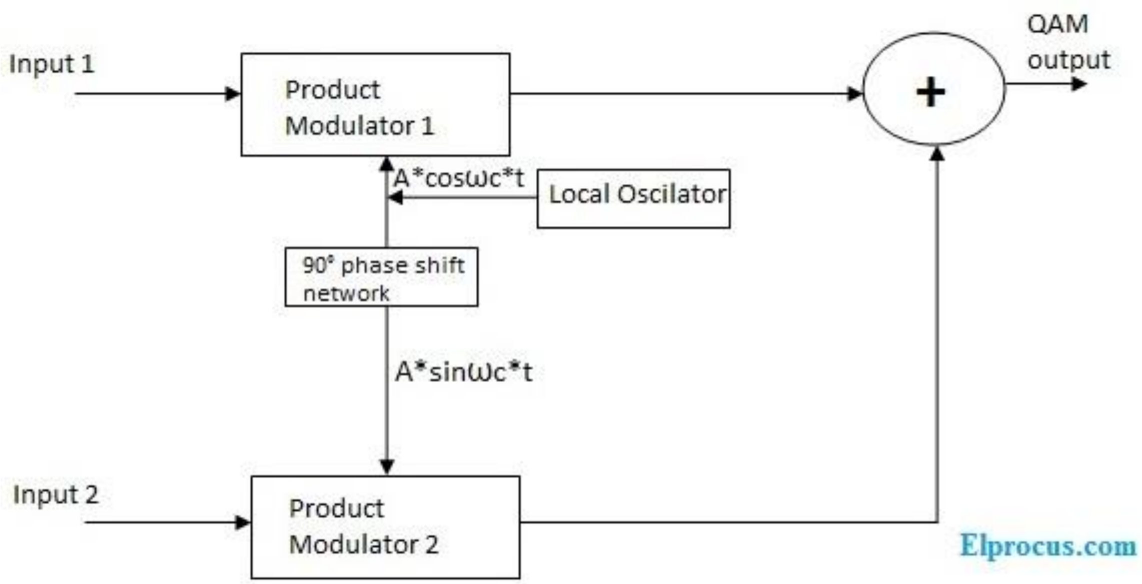
**Ans:**

| **Parameter** | **M-ary PSK** | **M-ary FSK** |
|---|---|---|
| **Number of bits per symbol** | N [$M = 2^N$] | N [$M = 2^N$] |
| **Symbol duration** | $T_S=NT_b$ | $T_S=NT_b$ |
| **Variable parameter** | Phase | Frequency |
| **Demodulation Method** | Coherent | Non-Coherent |
| **Bandwidth** | 2fb/N | 2 N+1fb/N |
| **Probability of Error** | More than that in M-ary FSK | Less than that in M-ary PSK |
| **Transmitted signal** | | |

**20. Draw the (a) Block diagram of QAM transmitter (b) Constellation diagram of 8 QAM. 6M**

**Ans:**

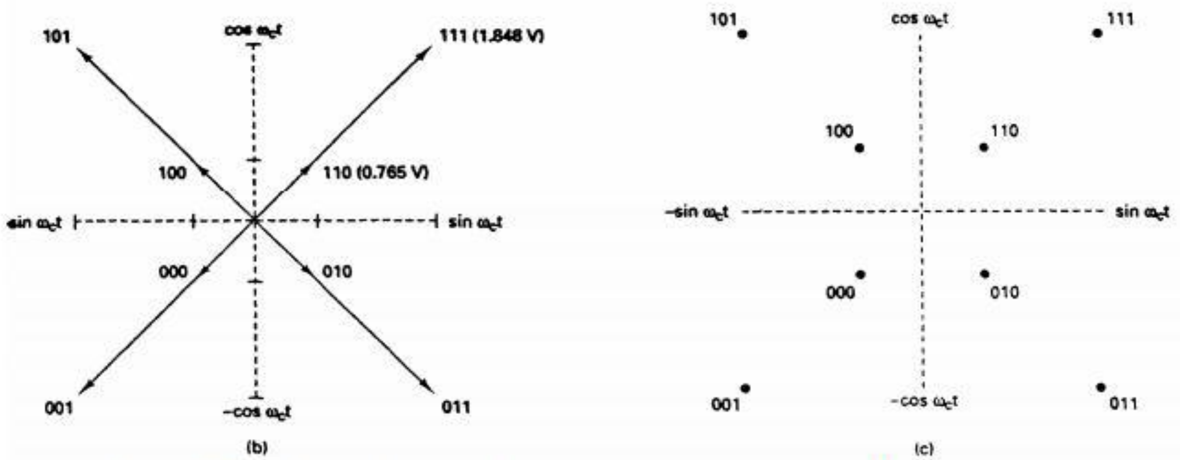
(a) Block diagram of QAM transmitter




(b) Constellation diagram of 8 QAM

| Binary input | | | 8-QAM output | |
|---|---|---|---|---|
| Q | I | C | Amplitude | Phase |
| 0 | 0 | 0 | 0.765 V | −135° |
| 0 | 0 | 1 | 1.848 V | −135° |
| 0 | 1 | 0 | 0.765 V | −45° |
| 0 | 1 | 1 | 1.848 V | −45° |
| 1 | 0 | 0 | 0.765 V | +135° |
| 1 | 0 | 1 | 1.848 V | +135° |
| 1 | 1 | 0 | 0.765 V | +45° |
| 1 | 1 | 1 | 1.848 V | +45° |

(a)

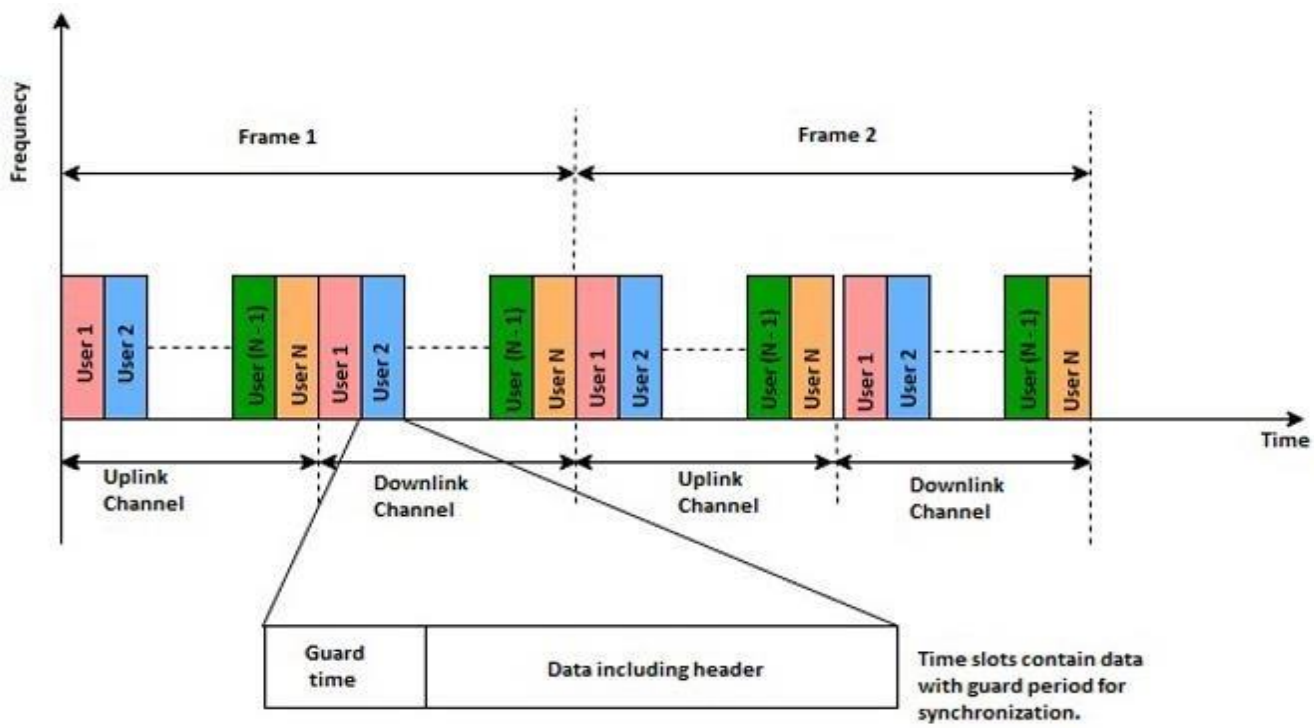



(a) truth table; (b) phasor diagram; (c) constellation diagram

# Unit 4 (12 M)

**21. Draw the block diagram of TDMA system and explain its working. 4M**

**Ans:**




In TDMA, the entire radio spectrum is divided into time slots and in each slot only one user is allowed to transmit or receive. Each user gets a cyclically repeating slot. When one user is transmitting it's information, the other users have to buffer their data i.e. TDMA users have to transmit data in a buffer and burst method, thus the transmission for any user is non-continuous.

As shown in Figure 3, A particular user gets time slots which are non continuous in nature. The next time slot is assigned to him/her only when the other users sharing the same spectrum have each done one burst of transmission atleast. Collection of time slots which are assigned to unique users is called as a *Frame*. In other words, a user gets only one time slot per frame to transmit.

**22. Compare TDMA and CDMA on the basis of sharing of time and B.W. Synchronization, code word, guard band and guard time. 4M**

**Ans:**

| **Features** | **TDMA** | **CDMA** |
|---|---|---|
| Sharing of time | It only shares the time of transmission through the satellite, not the channel. | It shares both time and bandwidth among multiple stations by allocating a unique code to each slot. |
| Bandwidth | Sharing of time of satellite Transponder using entire BW | Sharing of time and bandwidth both. |
| Synchronization | It requires synchronization. | It doesn't require any synchronization |

| | | |
|---|---|---|
| | | . |
| Code word | It doesn't require a codeword. | It needs a codeword. |
| Guard bands and guard times | It needed guard times. | It needed both guard times and guard bands. |

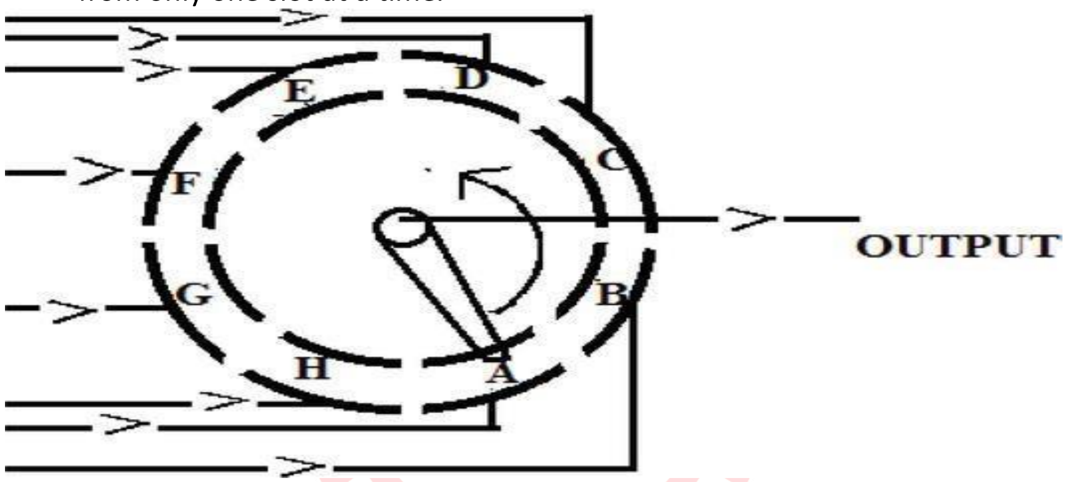
**23. Explain TDM technique with relevant diagram. 4M**

**Ans:**

- In time division multiplexing (TDM) all signals operate with the same frequency at different times, i.e., it is a technique of transmitting several signals over a single communication channel by dividing the time frame into equal slots.
- Here the signal transmitted can occupy the total bandwidth of the channel, and each signal will be transmitted in its specified time period only.
- In TDM all signal operates at same frequency at different time slots.
- Figure 8 shows the schematic diagram of implementation of TDM system. From this it is clear that a circular ring has been split into eight equal segments and is completely separated from one another.
- It is also noted that there is a movable arm attached to the inner

ring, and it slides over the eight segments over the ring.

- The eight segments are eight inputs, and the selector moves in clockwise direction from A to H; after completing one revolution, it starts again.
- The output is taken from the inner ring that contains the signal from only one slot at a time.




**24. Compare FDM & TDM systems (any four points). 4M**

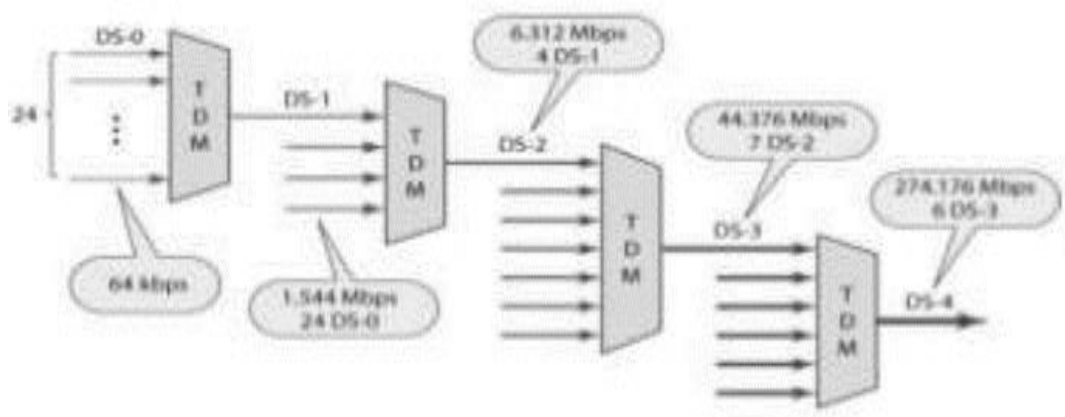
**Ans:**

| FDM | TDM |
|---|---|

| | |
|---|---|
| A technique that allows transmission of multiple signals using different frequency slots over a common link. | A technique that permits the flow of multiple data signal over a communication link in different time domains. |
| Frequency Division Multiplexing | Time Division Multiplexing |
| Analog | Digital |
| Not Needed | Necessary |
| Complex | Comparatively simple. |
| Exist | Does not exist |
| Not sensitive | Sensitive |
| Less | More efficient than FDM system |
| High | Comparatively low. |

**25. Describe North American (T-carrier) digital multiplexing hierarchy with neat diagram. 4M**

Ans:




**Explanation:-**

**T1 Carrier System**

T1 carrier systems were designed to combine PCM and TDM Techniques for the Transmission of 24 64Kbps channels with each channel Capable of Carrying Digitally. Encoded voice band telephone signals or data.
The transmission bit rate (line speed) for a T1 carrier is 1.544 Mbps.
All 24 DS-0 channels combined has a data rate of 1.544Mbps, this digital signal level is Called DS-1. Therefore T1 lines are referred as DS-1 lines.

**DS and T Line rates**

**T2 Carrier System**

T2 carriers time division multiplex 96 64-Kbps voice or data channels into a single 6.312 Mbps data signal for transmission over twisted pair copper wire up to 500 miles over a special metallic cable.

**T3 Carrier system**
T3 carriers Time division multiplex 672 64-kbps voice or data channels for transmission over a single coaxial cable. The transmission rate is 44.736 Mbps.

**T4 Carrier System**
T4 carriers time division multiplex 4032 64-kbps voice or data channels for transmitting over a single T4 coaxial cable upto 500 mile. The transmission rate is very high i.e.
274.16Kbps.

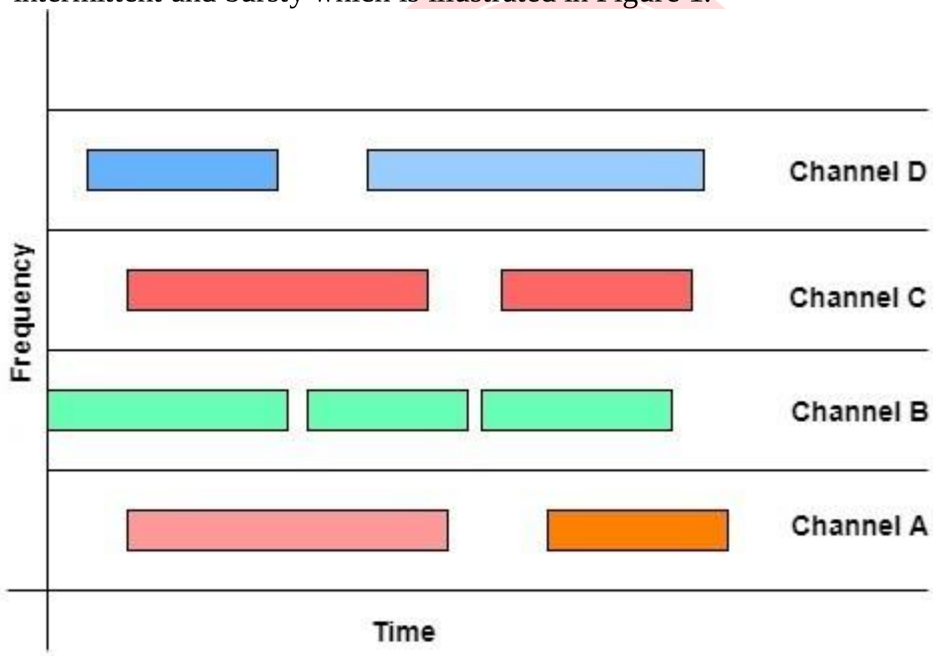
**T5 Carrier System**
T5 carriers time division multiplex 8064 64Kbps voice or data channels and transmit them at 560.16Mbps over a single coaxial cable.

| Service | Line | Rate (Mbps) | Voice Channels |
|---|---|---|---|
| DS-1 | T-1 | 1.544 | 24 |
| DS-2 | T-2 | 6.312 | 96 |
| DS-3 | T-3 | 44.736 | 672 |
| DS-4 | T-4 | 274.176 | 4032 |

## 26. Describe FDMA with suitable diagram.
**Ans:**

In FDMA, the entire spectrum is divided into narrow frequency channels and

then each unique channel is assigned to individual users. These channels are assigned on demand of users. During the period of the call, no other user can share the same channel. In FDMA/FDD systems, which are more common, each user is assigned a channel as a pair of frequencies; one is used for the forward channel while the other is used for the reverse channel.
The technical definition of the FDMA system is given as
As shown in Figure 1, the entire spectrum is divided into four channels named as channel A-D. Each channel is allotted to a single unique user. The user does not use the channel for the entire time interval as in a two way communication, one user cannot speak for more than 60 - 70 %% on an average. Hence traffic is intermittent and bursty which is illustrated in Figure 1.




- **Features**

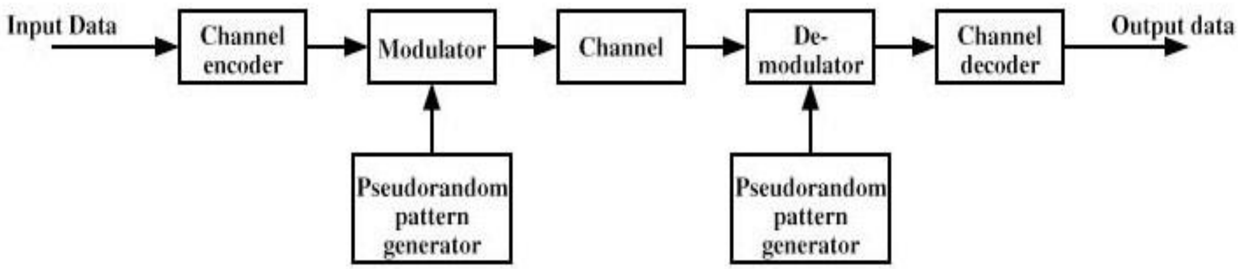
1. The FDMA channel carries only one phone circuit at a time. (one channel to one user)

2. When the FDMA channel is not in use then it sits idle and cannot be used by other users to increase or share capacity. It is essentially a wasted resource.
3. The Bandwidth of FDMA channels are relatively narrow (30 KHz in AMPS) i.e. it is used in narrow band systems.
4. The symbol time of a narrow band signal is large as compared to the average delay spread. Hence Intersymbol interference (ISI) is less. FDMA signals are more prone to flat fading.
5. Little or no equalization is required in FDMA narrowband systems.
6. Since FDMA is a continuous transmission scheme fewer bits are needed for synchronization.
7. FDMA systems have a higher cell site system costs as compared to TDMA systems.
8. FDMA requires tight RF filtering to reduce adjacent channel interference and intermodulation frequencies (which are explained in next section).
9. Adjacent channel interference is more due to non linear effects in FDMA system.

# Unit 5 (8 M)

**27. Explain with the help of block diagram, spread spectrum modulation system. 4M**

**Ans:**




The block diagram of spread spectrum digital communication is shown in above fig. the basic elements of a spread spectrum digital communication system with a binary information sequence at its input at the transmitting end and its output at the receiving end.

Functions of each block:

- Channel encoder : The channel encoder adds some redundant bits to the input bit sequence in properly defined format.
- Pseudorandom generator : It produced a pseudorandom or pseudonoise binary valued sequence.
- Modulator : Pseudonoise (PN) binary valued sequence is impressed on the transmitted signal at modulator.
- Channel : Medium through which signal travels towards receiver.
- Demodulator : The impressed PN sequence removed from the received signal at the demodulator.
- Channel decoder : The decoder at the receiver uses the coded bits to reconstruct error free accurate bit sequence and reduce the effects of channel noise and distortion.

**28. Differentiate between direct sequence spread spectrum and frequency hopped spread spectrum. 6M**

**Ans:**

| FHSS | DSSS |
|---|---|
| FH systems use a radio carrier that "hops" from frequency to frequency in a pattern known to both transmitter and receiver. | DS systems use a carrier that remains fixed to a specific frequency band. |
| Abroad,slice,of,the,bandwidth,spectrum,is, divided,into,many,possible,broadcast frequencies. | The data signal is spread onto a much larger range of frequencies (at a much lower power level) using a specific encoding scheme. |
| Frequencies are randomize | Frequency is constant |
| Data is constant | Data are randomize |
| Resistance to noise | Less resistant to noise |
| Limited throughput (2-3 Mbps @ 2.4 GHz) | Much higher throughput than FH (11 Mbps) |
| Systm,generate wideband signals controlled by commanding the carrier frequency,(frequency hopping) | Syestem,generate wideband signals controlled by the code is direct carrier,modeulation (direct sequence) |
| Frequency-hopping,devices,use,less,power,and,are,cheaper | Performance of DS-CDMA systems is usually,better and more reliable. |
| FHSS are significantly less sensitive to Bluetooth interference. | Though bandwidth efficiency decreases; reliability, integrity and security increase. |
| FHSS systems operate with SNR (Signal to Noise Ratio) of about 18 dB | DSSS systems, because of the more efficient modulation technique used (PSK), can operate with SNR as low as 12 dB |
| FHSS spreads the signal by hopping from one frequency to another across a bandwidth of 83 Mhz. | DSSS spreads the signal by adding redundant bits to the signal prior to transmission which spreads the signal across 22 Mhz |

| | |
|---|---|
| To some other receiver, FHSS appears to be a short-duration impulse noise. Thus, the data security increases | To,some other receiver, DSSS appears as low-power, wideband noise and is,rejected. |

**29. Explain direct sequence spread spectrum (DSSS) transmitter with block diagram.4M**

## Ans:

In a CDMA system, the narrowband message signal is multiplied with a very large bandwidth signal called as the spreading signal. The zeroes and ones of this spreading signal are called chips. It is basically a pseudo noise code sequence that has a chip rate which is very high as compared to the data rate of the message. This PN code is unique for every user. This PN code is orthogonal to the other codes, hence interference between users is minimized. With this arrangement, many users can use the same carrier frequency and can transmit simultaneously. The receivers need to know the code word of the corresponding sender to detect it.

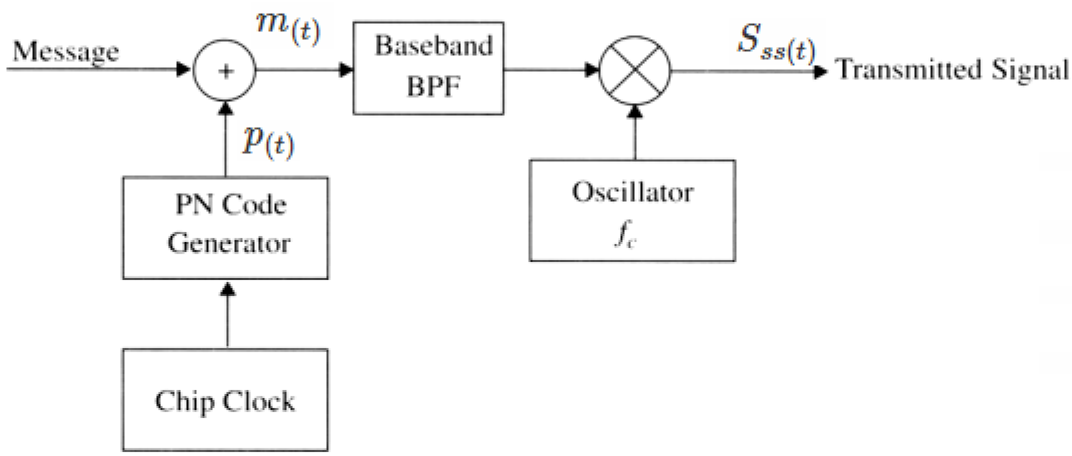
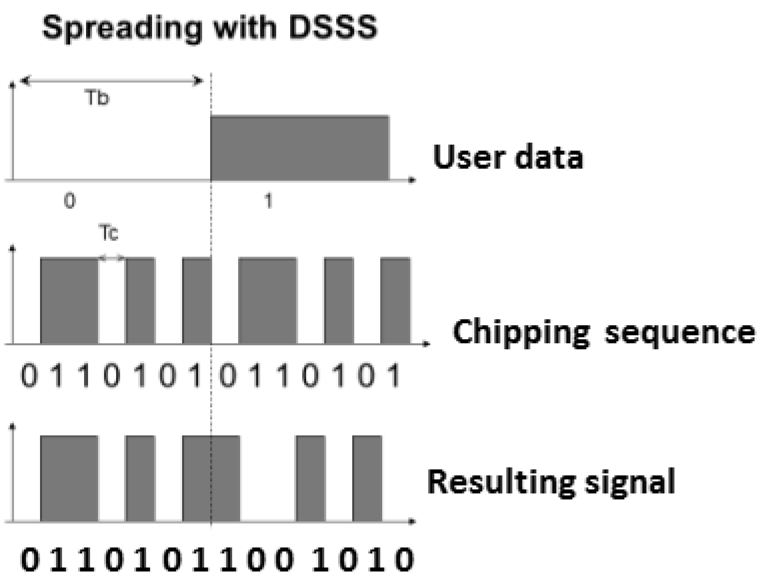



Figure 7 shows the DSSS transmitter system. As shown in Figure 7, the message signal is directly modulo-2 added with the PN code.

The process of coding can be explained as follows as illustrated in Figure 8,




Suppose, the user data m(t) is 0 and 1. let us assume that a 7 chip length code (chipping sequence) of 0110101 is repetitively used. Modulo 2 addition ( XOR operation ) is performed on the PN code p(t) with each bit of the data to be sent.

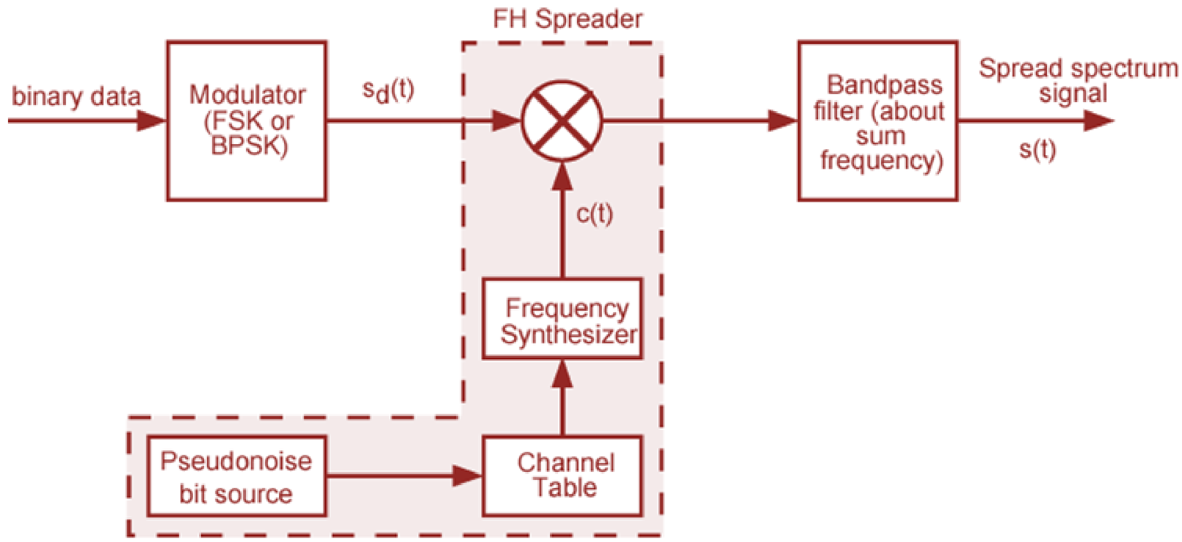
Data bit 0 with 0110101 gives the resultant as 0110101. Data bit 1 with the same code gives the resultant as 1001010. This coded sequence is then fed for further processes to a band pass filter, modulated on to a carrier frequency fc and then DSSS signal Sss(t) is transmitted.

**30. Explain Frequency hop spread spectrum (FHSS) transmitter with block diagram.4M**
**Ans:**

- Frequency-hopping spread spectrum (FHSS) is a method of transmitting radio signals by rapidly changing the carrier frequency among many distinct frequencies occupying a large spectral band. The changes are controlled by a code known to both transmitter and receiver. FHSS is used to avoid interference, to prevent eavesdropping, and to enable code-division multiple access (CDMA) communications.

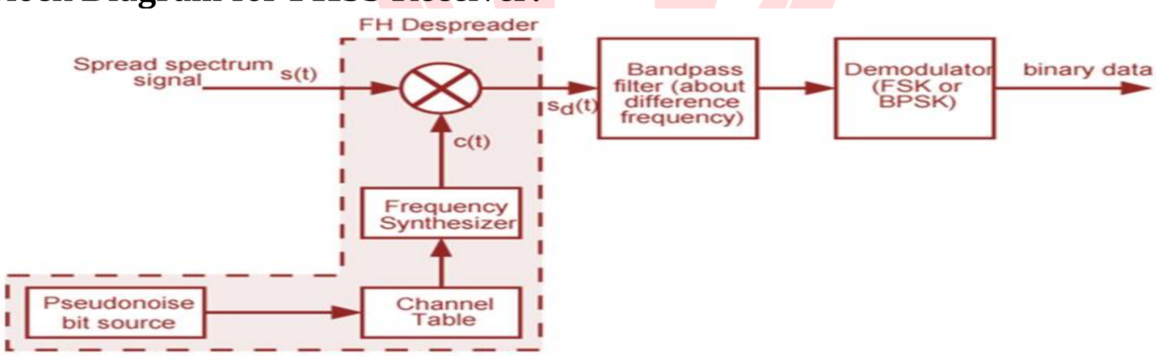
- With frequency hopping spread spectrum (FHSS), the signal is broadcast over a seemingly random series of radio frequencies, hopping from frequency to frequency at fixed intervals. A receiver, hopping between frequencies in synchronization with the transmitter, picks up the message. Would-be eavesdroppers hear on ly unintelligible blips. Attempts to jam the signal on one frequency succeed only It knocking out a few bits of it.
- FHSS is a method of transmitting radio signals by rapidly switching a carrier among many frequency channels, using a pseudorandom or pseudonoise sequence known to both transmitter and receiver.
- The advantage of this system is that the signal sees a different channel and a different set of interfering signals during each hop.
- This system helps to avoid the problem of failing communication at a particular frequency, because of a fade or a particular or unintentional interference.
- It is utilized as a multiple access method in the frequency-hopping *Code Division Multiple Access (FH-CDMA)* schemes.
- FHSS is also useful to counter eavesdropping, as well as to obstruct the frequency jamming of telecommunications

**Block Diagram for FHSS Transmitter:**




**FHSS Transmitter**

## Block Diagram for FHSS Receiver:




**FHSS Receiver**

- The above figure shows the Block diagram of the FHSS system for both transmitter and receiver.

- For transmission, binary data are fed into a modulator using some digital-to-analog encoding scheme, such as *Frequency Shift Keying (FSK) or Binary Phase Shift Keying (BPSK).*
- A PN source serves as an index into a table of frequencies each K bit on the PN source specifies one of the 2k carrier frequencies.
- At each successive interval, a new carrier frequency is selected.
- This frequency is then modulated by the signal produced from the initial modulator to produce a new signal with the same shape.
- On reception, the spread spectrum signal is demodulated using the same sequence of PN-derived frequencies and then demodulated to produce the output data.